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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,801	09/29/2000	Jeffrey L. Rabe	042390.P9428	8877

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BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN
7th Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025

EXAMINER	
PHAN, RAYMOND NGAN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/675,801	RABE ET AL.	
	Examiner	Art Unit	
	Raymond Phan	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This action is responsive to the following communications: amendment filed on June 18, 2004.

2. This application has been examined. Claims 1-18 and 31-60 are pending.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10, 14-15, 31-60 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bashford (US No. 6,629,179) in view of Pawlowski (US No. 5,956,516).

In regard to claims 1, 4, 7, 10, Bashford discloses method comprising the step of receiving an interrupt (see col. 7, lines 8-61); converting the interrupt into an upstream memory write interrupt (see col. 7, line 8 through col. 8, line 6) by generating a memory write request to a predetermined address of a memory space (see col. 1, line 60 through col. 2, line 10). But Bashford does not specifically disclose the converting the upstream memory write interrupt into a front side bus (FSB) interrupt transaction, wherein one or more processors coupled to the FSB are capable of receiving the FSB interrupt as a part of a FSB transaction. However Pawlowski discloses the converting (i.e. decoding) the upstream interrupt into a front side bus (FSB) interrupt transaction (see col. 4, lines 23-60), wherein one or

more processors coupled to the FSB are capable of receiving the FSB interrupt as a part of a FSB transaction (see col. 4, line 61 through col. 5, line 5). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Pawlowski within the system of Bashford because it would reduce the wait times for service of interrupts.

In regard to claims 2, 5, 8, Bashford discloses wherein the interrupt is generated by a PCI device (see col. 7, lines 8-61).

In regard to claims 3, 6, 9, Pawlowski discloses wherein the FSB interrupt is received by the processor (see col. 4, lines 23-60).

In regard to claim 14, Bashford discloses the interrupt is generated by the PCI device (see col. 4, lines 31-44) and wherein the chipset is coupled to the processor (see figure 1).

In regard to claims 31, 34, 37, 44, 51, 59, Bashford discloses the method comprising receiving, at an I/O controller, an interrupt request from an I/O device (see col. 5, line 30 through col. 6, line 22); generating, at the I/O controller, a memory request at the predetermined address in the response the interrupt request (see col. 1, lines 60 through col. 2, line 10); transmitting the memory request to the memory, the memory request being processed at the memory controller as one or more memory cycles (see col. 5, line 30 through col. 6, line 22). But Bashford does not specifically disclose memory request is being routed to a coupling with one ore more processors as a part of one or more interrupt message transactions on the bus. However Pawlowski discloses memory request is being routed to a coupling with one ore more processors as a part of one or more interrupt message transactions on the bus (see col. 4, lines 16-60). Therefore, it would have been

obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Pawlowski within the system of Bashford because it would it would reduce the wait times for service of interrupts.

In regard to claims 32, 52, Bashford discloses wherein the memory request is a memory write request to the memory controller (see col. 5, line 30 through col. 6, line 22).

In regard to claims 33, 38, 44, 53, Bashford discloses wherein the interrupt request is one of the interrupt request hardware signal and a memory write request to the I/O controller (see col. 5, line 30 through col. 6, line 22).

In regard to claims 39, 46, 54, Bashford discloses wherein the memory request is received one or more I/O device coupled to the memory controller (see col. 5, line 30 through col. 6, line 22).

In regard to claims 40, 47, 55, Pawlowski et al. disclose wherein the interrupt is marked as lowest priority re-directable and redirected to the lowest priority register (see col. 4, line 16 through col. 5, line 40).

In regard to claims 41, 48, 56, Pawlowski et al. disclose redirecting at least one interrupt based on the task priority information (see col. 5, line 6 through col. 6, line 20).

In regard to claims 42, 49-50, 57-58, Pawlowski e al. disclose further comprising providing support for the updated TPR transactions to update at least one updated TPR register (see col. 5, line 6 through col. 6, line 20).

In regard to claim 43, Pawlowski et al. disclose wherein the processor has the lowest priority among one or more processors (see col. 5, line 6 through col. 6, line 20).

In regard to claim 60, Pawlowski et al. disclose redirecting at least one interrupt based on the task priority information (see col. 4, lines 45-64) and providing support for the updated TPR transactions to update at least one updated TPR register (see col. 7, line 51 through col. 8, line 14).

11. Claims 11-13 and 16-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bashford in view of Pawlowski and further in view of Tyner (US No. 6,564,276).

In regard to claim 11, Bashford and Pawlowski disclose the claimed subject matters as discussed above rejections except the teaching of the chipset comprising at least one I/O controller hub (ICH), P64H, and AGP device. However Tyner specifically discloses the chipset comprising at least one I/O controller hub (ICH) 115, P64H 114, and AGP device 110 (see figure 1). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Tyner within the system of Bashford and Pawlowski because it would provide various controllers and functions within the chipset.

In regard to claim 12, Pawlowski discloses the I/O component of an APIC configured to convert the interrupt into the upstream interrupt (see col. 2, lines 45-64). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Pawlowski within the system of Bashford and Tyner because it would reduce the wait times for service of interrupts.

In regard to claims 13, 16, Tyner discloses the chipset comprising a HUB interface coupled to the first end of IOxAPIC and coupled to the second end to

MCH (see col. 3, lines 7-63). But Tyner does not specifically disclose wherein the memory control hub configured to convert the upstream interrupt into the FSB interrupt transaction. However Pawlowski disclose the converting (i.e. decoding) the upstream interrupt into a front side bus (FSB) interrupt transaction (see col. 4, lines 23-60). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Pawlowski within the system of Bashford and Tyner because it would reduce the wait times for service of interrupts.

In regard to claim 17, Pawlowski discloses wherein the routing mechanism configured to flush the upstream interrupt before propagating an interrupt upstream (see col. 4, lines 16-60).

In regard to claim 18, Pawlowski discloses wherein the interrupt controller receive the EOI from the processor and broadcast the EOI to at least one device (see col. 6, lines 40-55).

Response to Arguments

5. In view of amendment and remarks filed on June 18, 2004, claims 1-60 have been fully considered but they are not deemed to be persuasive.

Applicant(s) argue that ...Bashford fails to teach or suggest to generate a memory write request to a predetermined address of a memory space... (page 11). The Examiner does not agree. Bashford teaches the step of generating a memory write request to a predetermined address of a memory space (see col. 1, line 60 through col. 2, line 10).

Applicant(s) argue that ...Pawlowski fails to teach or suggest to convert an upstream interrupt into a host bus interrupt... (page 12). The Examiner does not agree. Pawlowski teaches wherein one or more processors coupled to the FSB are

capable of receiving the FSB interrupt as a part of a FSB transaction (see col. 4, line 61 through col. 5, line 5).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., generating a memory write request to a predetermined address of a memory space and/or wherein one or more processor coupled to the FSB are capable of receiving the FSB interrupt as part of the FSB transaction) are not recited in the rejected claims 10, 31, 34, 37. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. *In re Van Glens*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

6. All claims are rejected.

7. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Bennett (US No. 6,466,998) discloses an interrupt routing mechanism for routing interrupts from peripheral bus to interrupt controller.

Haren (US No. 6,694,392) discloses a transaction partitioning.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (703) 306-2756. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (703) 305-9656 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (703) 746-7239.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**raymond.phan@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

RP

Raymond Phan
9/17/04